In the Specification:

Please amend the paragraph at page 1, lines 3-8, as indicated below.

The present invention is related to and fully incorporates the subject matter disclosed in concurrently-filed U.S. Patent Applications, No. 09/[[____,____]]871,197, entitled "Parallel Communication Based On Balanced Data-Bit Encoding" (VLSI.295PA), No. 09/[[____,____]]871,160, entitled "Parallel Data Communication Consuming Low Power" (VLSI.299PA), and No. 09/[[____,____]]871,117, entitled "Parallel Data Communication Having Multiple Sync Codes" (VLSI.312PA).

Please amend the paragraph at page 5, lines 5-8, as indicated below.

FIGs. 1-1 through 1-4 are[[is]] a diagram of an example parallel data communication arrangement in which digital data is transferred in parallel from a first module to a second module over a communication channel including a plurality of parallel data-carrying lines, according to the present invention; and

Please amend the paragraph at page 5, lines 9-10, as indicated below.

FIGs. 2-1 through 2-2 are[[is]] a diagram of another example parallel data communication line arrangement, also according to the present invention.

Please amend the paragraph at page 5, line 19 – page 6, line 2, as indicated below.

The present invention is believed to be generally applicable to methods and arrangements for transferring data between two modules (functional blocks) intercoupled by a parallel data communication path. The invention has been found to be particularly advantageous for high-speed data transfer applications susceptible to data-skew errors. Examples of such applications include, among others: SSTL (stub series transceiver/terminated logic); RSL (Rambus Signaling Logic) interfaces; closely-connected applications such as where the parallel data communication path intercouples the two modules on a single-chip; and off-board high-speed communication between chips typically situated immediately adjacent each other on the same printed circuit board. A specific example of an off-board high-speed communication between chips is described in U.S. Patent Application Serial No. 09/215,942, filed on December 18, 1998, now U.S. Patent No.

[[_____]]6,347,395, incorporated herein by reference. While the present invention is not necessarily limited to such applications, an appreciation of various aspects of the invention is best gained through a discussion of examples in such an environment.

Please amend the paragraph at page 7, lines 11-19, as indicated below.

FIGs. 1-1 through 1-4, collectively FIG. 1, illustrate[[s]] a parallel-data communication line arrangement 100, according to another example embodiment of the present invention. The arrangement 100 includes a differential clock that is used to define the rate at which the data is synchronously passed between from a processing circuit, such as CPU 102 and registers 106, at sending module 112 to a receiving module 114. The skilled artisan will appreciate that a differential clock is not required for all applications, and that although FIG. 1 illustrates the data being passed in only one direction, reciprocal communication can also be provided with each of the modules 112 and 114 being part of a respective communication node including the reciprocal set of transmit and receive circuits.

Please amend the paragraph at page 8, lines 29 – page 9, line 7, as indicated below.

FIGs. 2-1 through 2-2, collectively FIG. 2, illustrate[[s]] another implementation of the present invention in which six of the same types of encode/decode clock domain circuits of FIG. 1 are used in each of two communication paths for communication in each respective direction. For passing communications initiated at a first terminal 210 for reception at the second terminal 212, one of the six identical clock domain circuits is depicted by connected circuits 216a and 216b. For communications initiated at the second terminal 212 for reception at the first terminal 210, six additional encode/decode clock domain circuits of this type are used; one of these circuits is depicted by connected circuits 236a and 236b. For the sake of brevity, the following discussion is limited to the communication flow initiated at the first terminal 210 for reception at the second terminal 212.